CLAIMS

1. A folded starved inverter differential output apparatus for use in a voltage controlled oscillator comprising:

a first polarity of two transistors cross-coupled;

a second polarity of four transistors;

two inverter gates; and

a supply regulator.

2. A folded starved inverter differential output apparatus of claim 1 wherein the second polarity of four transistors are connected to perform input and control functions.

3. A folded starved inverter differential output apparatus of claim 2 wherein first polarity can be positive or negative

4. A folded starved inverter differential output apparatus of claim 2 wherein the inverter gates provide linearity to an output voltage.

5. A folded starved inverter differential output apparatus of claim 2 wherein the supply regulator reduces power supply fluctuations.

6. A folded starved inverter differential output apparatus of claim 5 wherein the first polarity of cross-coupled transistors is connected to provide a differential generating output voltage.

7. A folded starved inverter differential output apparatus comprising

two transistors cross-coupled to provide an output stage;

four transistors connected to provide a folded starved inverter circuit;

two inverter gates; and

a supply regulator; wherein the folded starved inverter differential output apparatus provides a fast slew rate, large voltage swing and symmetric output waveform.

8. A folded starved inverter differential output apparatus of claim 7 wherein the cross-coupled transistors provide a differential output.

9. A folded starved inverter differential output apparatus of claim 7 wherein the inverter gates provide linearity to the output voltage.

10. A folded starved inverter differential output apparatus of claim 7 wherein the supply regulator reduces power supply fluctuations.

11. A folded starved inverter differential output apparatus of claim 7 wherein two of the four transistors provide an input connection.

12. A folded starved inverter differential output apparatus of claim 7 wherein two of the four transistors provide a current controlling function

13. A receiver apparatus comprising:

a phase locked loop circuit including a voltage controlled oscillator used to generate a data sampling clock signal;

a data sampler to receive the data sampling clock signal; and

a folded starved inverter circuit contained within the voltage controlled oscillator.

14. A receiver apparatus of claim 13 wherein the folded starved inverter circuit provides a delay to an input signal.

15. A receiver apparatus of claim 14 wherein the folded starved inverter circuit contains two transistors cross-coupled to provide a differential output stage.

16. A receiver apparatus of claim 15 wherein the folded starved inverter circuit contains four transistors connected to provide a folded starved inverter circuit.

17. A receiver apparatus of claim 16 wherein two of the four transistors provide an input connection.

18. A receiver apparatus of claim 17 wherein two of the four transistors provide a current controlling function.

19. A receiver apparatus of claim 18 wherein the receiver further comprises a frequency comparator.

20. A receiver apparatus of claim 19 wherein the receiver samples received data at 3 times the frequency of the data signal.